REMARKS

Claims 1-3, 5 and 7-11 are pending in this application, claim 6 having been removed by amendment. The Examiner has rejected all pending claims as anticipated under 35 U.S.C. § 103(a) by Japanese Patent No. 50-14540A to Yoshida et al. ("Yoshida") in view of U.S. Patent No. to Howard et al.

In rejecting the claims as anticipated, the Examiner alleges that Yoshida teaches and discloses all of the elements of claim 1 of the present application, except that Yoshida does not disclose the limitation that "said control means controls said first bus and said second bus independently" or "the first bus is not connected to said display means" as recited in claim 1.

In the present invention, when a controller performs fast access to the memory by a first bus, the second bus which is controlled independently of said first bus, is not affected. Further, the display disposed in a vicinity of the antenna is connected to a second bus, such that when a controller performs fast access to the memory by a first bus, the antenna is not affected by the noise generated from the first bus because of first access. Other than, in Fig. 1 of Yoshida, there is no description about the memory. Therefore, the bus 40 (Fig. 1) of Yoshida is different from a first bus of the present invention. Further, the buses 40, 41 (Fig. 1) of Yoshida are formed independently, but, all component portions are connected to the respective buses 40, 41. Therefore, there is no description of "wherein said first bus is not connected to said display means, and said second bus is not connected to said storage means " of the present invention.

As recognized by the Examiner, in Yoshida, there is no disclosure or suggestion of "wherein said controller controls said first bus and said second bus independently" of the present invention. Further, the Video Bus 325 of Howard is not connected to the CPU 320 or connected to the system bus 310. Therefore, it is different from a second bus connected to said controller and said display of the present invention. Further, the system bus 310 and the Video Bus 325 of Howard are connected to the memory (VRAM). Therefore, there is o disclosure or suggestion of "wherein said first bus is not connected to said display, and said second bus is not connected to said memory" of the present invention.

Claim 7

Claim 7 contains the same limitations of a "first bus is not connected to said display, and said second bus is not connected to said storage means" as Claim 1, and therefore would not be obvious to one skilled in the art in light of Yoshida alone or in combination with Howard.

Claims 2-3, 5, and 8-11

Claims 2-3 and 5 depend from Claim 1 and Claims 8-11 depend from Claim 7, and are therefore patentable over Yoshida in combination with Howard for the same reasons as Claims 1 and 7.

For at least the reasons set forth above, Applicants respectfully submit that this patent application is in condition for allowance. The Examiner is urged to telephone Applicants' undersigned counsel at the number provided below if it will advance the prosecution of this application. Reconsideration and prompt allowance of this patent application are respectfully requested.

Respectfully submitted,

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